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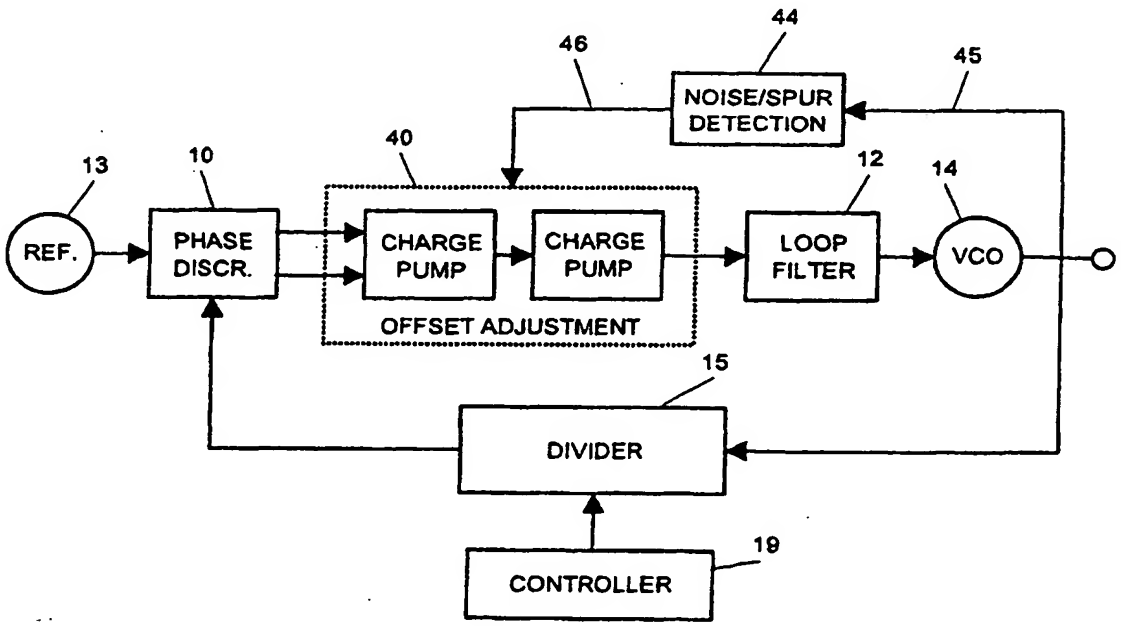

(57) Abstract

Phase lock loop systems in which a phase offset is introduced between a reference signal (SR) and a loop signal (SO) to improve linearity. The phase offset is produced by a linearizing network (40) inserted in the phase lock loop between a phase discriminator (10) and a loop filter (12). The linearizing network (40), which may be part of a charge pump circuit (40) receives adjustment signals (46) according to characteristics of the phase lock loop output signal (45) or the loop signal (SO). For example, distortion or noise levels in these signals may be monitored or minimized.

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IMPROVEMENTS RELATING TO PHASE LOCK LOOPS

FIELD OF THE INVENTION

The present invention relates to phase lock loops (PLLs) and particularly but not solely to radio frequency (RF) synthesisers, amplifiers or other systems which incorporate PLLs. More particularly the invention relates to a system for improving linearity of the phase discriminator and charge pump combination which forms part of a PLL.

BACKGROUND TO THE INVENTION

Radio communication devices employ frequency synthesisers to control transmission and reception of signals. A synthesiser generally includes a reference oscillator which generates a stable reference frequency signal and is used to determine the output of a frequency controlled oscillator which in turn generates a variable RF output signal. This output signal is generally coupled to an antenna of the communication device by way of one or more mixers which modulate or demodulate the signal for transmission or reception respectively. The synthesiser is programmed by a control unit such as a digital processor to produce the controlled oscillator signal at a range of frequencies as required by the device.

Indirect frequency synthesisers use one or more PLLs to generate the variable output signal. The PLL contains a phase discriminator which generates an output according to the phase difference or phase error between the reference signal and a feedback signal. The feedback signal is generally produced by dividing the frequency of the output from the controlled oscillator. A charge pump arrangement receives the output from the discriminator and generates error correction pulses which are supplied to a loop filter. The loop filter provides a control signal for the controlled oscillator. Voltage rather than current controlled oscillators are normally used. Output from the oscillator may be amplified before or after feedback to the discriminator. In general terms, a type two PLL of this kind attempts to match the frequency of the controlled oscillator to a multiple of the reference frequency and stabilise with a predetermined phase difference between the reference and feedback signals.

Frequency division of the output of the frequency controlled oscillator can be implemented in various ways to enable a relatively low frequency reference to determine

a wide range of variable RF output. Integer-N techniques are limited to a range of discrete multiples of the reference frequency which is often satisfactory. Fractional-N techniques are also commonly used and allow a synthesiser to achieve relatively fine frequency resolution. Fractional techniques modulate the instantaneous divide ratio of the feedback to the phase discriminator but consequently may produce unacceptable spurious frequencies and phase noise in the synthesiser output. Various cancellation schemes such as phase interpolation have been employed to reduce the fractional spurs and noise but generally require an increase in complexity and cost of the synthesiser to achieve a significant reduction in amplitude of the spurs.

Fractional-n synthesisers which use sigma-delta modulation to reduce phase noise and spurs resulting from non-integer division ratios are well known, as described in US 4,609,881 for example. The phase discriminator in a fractional-n synthesiser acts as a digital-to-analog converter for the sigma-delta modulation. It is also well known that the converter must be highly linear in order to maintain the noise-shaping benefits of the modulator, as described for example, in "Oversampling methods for A/D and D/A conversion", Oversampling delta-sigma converters, IEEE Press 1992. If operation of the phase discriminator is non-linear then noise and fractional spurs can be reintroduced.

The PLL in a conventional radio synthesiser, amplifier or other arrangement operates to minimise the phase difference between the reference signal and the feedback signal at the input to the phase discriminator. The loop is said to be locked when the phase difference reaches 0° or a predetermined phase offset from 0°. Operation at 0° leaves the loop prone to dead zones near zero which arise due to existing non-linearities in the discriminator and particularly when the time span of the phase difference is appreciably smaller than the turn-on time of the charge pump arrangement. In a dead zone the charge pumps do not turn fully on and the amount of charge delivered to the loop filter changes non-linearly with the phase difference.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a system for improving the linearity of phase discrimination and corresponding control of the variable frequency output in a phase locked loop. Linearity is improved generally by modifying operation of the PLL so that the reference and feedback signals which are input to the discriminator are offset by a selected non-zero phase difference.

Accordingly in one aspect the invention may broadly be said to consist in a phase lock loop system including: phase discriminator means which generates a frequency change signal according to phase differences between a reference signal and a loop signal, oscillator means which generates an output signal in response to the frequency change signal, feedback means which couples the output signal to the discriminator means to form the loop signal, and adjustment means which introduces a phase offset between the reference signal and the loop signal according to characteristics of the output signal or the loop signal.

In another aspect the invention consists in a phase lock loop including: a phase discriminator which receives a reference signal and a loop signal and provides an up signal when the loop signal phase lags the reference signal phase and a down signal when the loop signal phase leads the reference signal phase, a first charge pump which provides a first current action in response to the up signal and a second current action in response to the down signal, being substantially opposed current source and current sink actions, a second charge pump which combines a third current action with the first and second current actions to add a phase offset between the reference signal and the loop signal, a charge accumulator which provides a frequency control signal in response to the combined first, second and third current actions of the first and second charge pumps, an oscillator which provides an output signal at a frequency in response to the control signal and is coupled to the phase discriminator to provide the loop signal, and an offset adjuster which varies one or more of the first, second or third current actions to vary the phase offset in accord with characteristics of the loop signal or characteristics of the output signal.

In a third aspect the invention consists in a phase lock loop including: a phase discriminator which receives a reference signal and a loop signal and provides an up signal when the loop signal phase lags the reference signal phase and a down signal when the loop signal phase leads the reference signal phase, a first charge pump which provides a first current action in response to the up signal and a second current action in response to the down signal, being substantially opposed current source and current sink actions, a second charge pump which provides a third current action having a magnitude substantially proportional to that of the first or second current action to add a predetermined phase difference between the reference signal and the loop signal, a charge accumulator which provides a frequency control signal in response to the combined first,

second and third current actions of the first and second charge pumps, and an oscillator which provides an output signal at a frequency in response to the control signal and is coupled to the phase discriminator to provide the loop signal.

BRIEF LIST OF FIGURES

Preferred embodiments of the invention will be described with reference to the accompanying drawings of which:

Figure 1 schematically shows a conventional phase lock loop arrangement including a phase discriminator and charge pump,

Figure 2 indicates phase adjustment signals output by the phase discriminator for the charge pump in Figure 1,

Figure 3 indicates how non-linearity can arise in the output of the charge pump,

Figure 4a schematically shows a PLL arrangement having a lineariser for adjustment of phase offset,

Figure 4b shows a PLL having a phase offset adjustment determined by characteristics of the loop signal,

Figure 4c shows a PLL having a phase adjustment determined by characteristics of the output signal,

Figures 5 and 6 indicate phase adjustment signals output by the phase discriminator, and

Figures 7 and 8 are example charge pump circuits for phase adjustment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to these figures it will be appreciated that a PLL according to the invention can be implemented in various ways and for various purposes within the scope of the claims. The preferred embodiments relating to frequency synthesisers are described by way of example only. The known components of PLL and synthesiser devices will be understood by a skilled person and a detailed explanation of their function need not be given.

Figure 1 shows a conventional frequency synthesiser using a PLL as a feedback control system. The PLL contains a phase discriminator 10, charge pump arrangement 11, loop filter 12, a reference oscillator 13 and a voltage controlled oscillator (VCO) 14. A programmable frequency divider 15 is included in a feedback path 16 from the VCO to the phase discriminator. The discriminator compares the frequency f_r of the signal SR

from the reference oscillator with the frequency f_0 of the signal SO from the VCO after division by N. It generates output signals FU and FD for the charge pump arrangement which provide a measure of the phase difference between these signals. If the phase of signal SR leads the phase of signal SO then the output FD is a frequency down signal on line 17 which serves to decrease the frequency of the VCO. If the phase of signal SR lags that of signal SO then the output FU is a frequency up signal on line 18 which serves to increase the frequency of the VCO. In normal operation the PLL stabilises so that signals SO and SR have zero phase difference at the discriminator, and the output of the VCO forms the output of the synthesiser with a frequency given by $f_0 = N f_r$. A controller 19 modulates the divider and sets the value of N.

Figure 1 also shows a conventional charge pump arrangement 11 having two opposed pumps which are typically in the form of a current source 30 and a current sink 31. The phase discriminator 10 provides a frequency adjustment signal on lines 17 and 18 in the form of two signals FU and FD which activate respective pumps in the arrangement. Each pump produces a respective current action which delivers charge to or extracts charge from the loop filter 12 which is effectively a charge accumulator. The loop filter accumulates charge in response to the pumps and generates a frequency control signal on line 32, typically in the form of a voltage level which controls the frequency of output from the VCO 14. The charge pumps and loop filter may together be considered as a control arrangement which couples the discriminator to the VCO. The charge pumps may alternatively be considered as part of the discriminator 10 in some arrangements.

Figures 2a, 2b, 2c and 2d indicate operation of the phase discriminator 10 in more detail. They respectively set out idealised input signals SR from the reference oscillator 13 and SO from the VCO 14 via programmable frequency divider 15, and idealised output signals FU and FD to the charge pump 11 on lines 17 and 18. The figures are arranged to demonstrate three distinct Cases of operation I, II, III in which SR is in phase with SO, leads SO, or lags SO respectively as shown. In this example the discriminator outputs a negative frequency down pulse on detection of an input pulse from the programmable divider and a positive frequency up pulse on detection of an input pulse from the reference oscillator. The frequency down pulse is terminated on detection of an input pulse from the reference oscillator, and the frequency up pulse is terminated on detection of an input pulse from the programmable divider. The output pulses have a minimum length according to the reset time t_r of output circuits in the discriminator.

Referring again to Figures 2a, 2b, 2c, 2d, in Case I the discriminator detects input pulses 20 and 21 simultaneously as the signals received from the reference oscillator and the programmable divider are in phase, and produces two output pulses 22 and 23 which have the minimum length. In Case II the signal SR leads signal SO so that the discriminator produces a long frequency up pulse 24 and a minimum frequency down pulse 25. In Case III the signal SR lags the signal SO so that the discriminator produces a relatively long frequency down pulse 27 and minimum frequency up pulse 26. The phase error between the input signals is indicated as t_e. Other types of pulsed operation are also possible.

Figure 3 indicates how non-linearity can arise through operation of the phase discriminator 10 and a charge pump arrangement 11 in a conventional PLL such as shown in Figure 1. The pump circuits 30 and 31 are controlled by signals FU and FD produced by the discriminator on lines 17 and 18 to in turn produce current pulses for the loop filter on line 32. Each pump has a turn on time t_{cp} which may be greater, approximately equal to, or smaller than the phase error t_e between SR and SO, as demonstrated by the current pulses A, B, C. The charge contained in each pulse delivered to the loop filter is intended to be proportional to the phase error, with the total charge being the integral of current on line 32 over time. The integral of current in Figure 3 is proportional to the area under the three pulses A, B, C for example. When the phase error is small relative to the turn on time the particular charge pump 30 or 31 may not turn fully on as indicated by pulse A. A non-linearity of this kind may also be attributable to the phase discriminator. It is only when the phase error becomes relatively greater than the turn on time that the pump turns fully on, as indicated by pulse C, and the area under the pulse is then proportional to the error. Accumulation of charge by the loop filter and control of the VCO is therefore non-linear until the phase error is approximately equal to the turn on time, as indicated by pulse B.

Figure 4a shows a frequency synthesiser with a linearised PLL. A lineariser 40 which modifies the output of a charge pump arrangement 41 is included in the control arrangement for the VCO 14. The lineariser acts to cause a predetermined adjustment of phase difference or offset between the signals SR and SO which are input to the phase discriminator 10. This additional phase difference or offset ensures that one of the charge pumps such as shown in the arrangement 11 of Figure 1 turns fully on to reduce the extent of non-linearity as described in relation to Figure 3. The PLL stabilises with a non-zero phase difference between SR and SO. Tests have indicated that phase noise and fractional spurs in the output of the synthesiser can be reduced for predetermined phase differences

greater than zero depending on details of the PLL arrangement, particularly the choice of sigma delta modulation and VCO. This effect may be due to coupling of signals or to ground bounce in the digital circuitry. A non-zero phase offset of an appropriate magnitude between 0° and ±90° causes the discriminator and charge pump arrangement to operate with improved linearity. A suitable value of the offset can be determined in various ways according to the invention, preferably in response to operating characteristics of the PLL itself, such as the output signal or a signal derived or otherwise associated with the output signal.

In Figure 4b a controller 41 which modulates the divider 15 also sets an appropriate value for the phase offset introduced according to the modulation. A range of suitable offsets could be provided in a lookup table, for example. The controller is connected to the lineariser 40 by line 46 and to the divider by line 47. The lineariser is shown as an overall offset adjustment which includes the charge pump arrangement and an additional charge pump. In Figure 4c a feedback controller 44 detects spurs in the output of the VCO 14 and continuously sets a value for the phase offset which reduces and ideally minimises the spurs. This controller is connected to the lineariser by line 46 and to the VCO by line 45. The controller 44 can operate according to various known algorithms involving detection of a characteristic in the output of the VCO. Detection and minimisation of distortion in the VCO signal, or out-of-band emissions, for example. Reference is made to *Electronics Letters:* Vol 34, No 22, p2093; Vol 31, No 3, p155; Vol 25, No 9, p576, which show techniques for sampling aspects of the output signal, or derivatives of the output signal. The search algorithm is easily modified to provide for desired phase control in each case.

Various networks which provide an offset adjustment according to the concepts set out in Figures 4b or 4c are envisioned. In radio amplification systems, such as used in LINC and EER transmitters, for example, a combination of two or more PLLs may be used to produce a single output signal. A characteristic of this single signal may be monitored and used to determine phase offset information for one or more of the PLLs.

Figures 5a, 5b, 5c and 5d indicate operation of the phase discriminator 10 of Figure 4 in more detail where SO leads SR by a predetermined phase difference. The figures are arranged to demonstrate three distinct Cases of operation I, II, III in which SO has stabilised in a fixed phase relationship with SR, and in which an additional phase error has arisen so that SO either lags or leads this predetermined difference. A time span t_p equal to the predetermined phase difference is indicated in addition to the reset time t_r of the

charge pumps. In each Case it can be seen that the length of the frequency up pulses in the signal FU vary around t_p and are generally greater than t_r. The charge pump 30 in Figure 1 would turn fully on under these circumstances and largely avoid non-linearity in the quantity of charge delivered to the loop filter 12. A sufficiently large phase error approaching t_p would temporarily reintroduce non-linearity and would occur only when sufficiently large changes of output frequency are required of the synthesiser. By careful selection of current sink 31 in Figure 1, lock times for positive and negative steps can be made substantially equal.

Figures 6a, 6b, 6c and 6d indicate alternative operation of the phase discriminator 10 of Figure 4 where SO lags SR by a predetermined phase difference. Once again the figures are arranged to demonstrate three distinct Cases of operation I, II, III in which SO has stabilised in a fixed phase relationship with SR, and in which an additional phase error has arisen so that SO either leads or lags this predetermined difference. A time span t_p equal to the predetermined phase difference is indicated in addition to the reset time t_r of the charge pumps. In each Case it can be seen that the length of the frequency down pulses in the signal FD vary around t_p and are generally greater than t_r. The charge pump 31 in Figure 1 would turn fully on under these circumstances and largely avoid non-linearity in the quantity of charge delivered to the loop filter 12. Again a sufficiently large phase error approaching t_p would temporarily reintroduce non-linearity and would occur only when sufficiently large changes of output frequency are required of the synthesiser.

Figure 7 shows a simple lineariser 40 and charge pump arrangement 41 which causes a predetermined phase difference between SO and SR as described in relation to Figures 5a, 5b, 5c, 5d. Figure 8 shows a simple lineariser which causes a phase difference as described in relation to Figures 6a, 6b, 6c, 6d. In each figure the lineariser preferably provides a charge pump in addition to those of the arrangement 41 although other networks may also be envisioned to achieve this purpose. A combination of simple linearisers such as shown in these figures might also be used. The additional charge pump in each case acts as a current sink or source to draw or transfer charge to or from the loop filter 12 at an appropriate rate on line 32. The linearisers 40 are simple bipolar transistor circuits connected to line 32 by line 42. Current sourced or sunk is set by a digital-to-analog converter DAC 75 which receives a control word on line 46 from controller 45. Alternatively a resistor divider having a divide ratio which sets the input to the base of bipolar transistor may replace the DAC. Many alternative circuits are possible for offset adjustment and those described here are given by way of example only.

CLAIMS:

1. A phase lock loop system including:

phase discriminator means which generates a frequency change signal according to phase differences between a reference signal and a loop signal,

oscillator means which generates an output signal in response to the frequency change signal,

feedback means which couples the output signal to the discriminator means to form the loop signal, and

adjustment means which introduces a phase offset between the reference signal and the loop signal according to characteristics of the output signal, the loop signal or an associated signal.

2. A system according to claim 1 further including:

detection means which monitors the output signal or a derivative of the output signal and determines a phase offset for the adjustment means to reduce noise or frequency spurs in the output signal.

3. A system according to claim 1 further including:

frequency division means in the feedback means which modulates the frequency of the loop signal and determines a phase offset for the adjustment means to reduce noise or frequency spurs in the output signal.

4. A system according to claim 1 wherein:

the phase discriminator means includes a charge pump arrangement having a plurality of pump actions at least one of which is varied by the adjustment means to introduce the phase offset.

5. A phase lock loop including:

a phase discriminator which receives a reference signal and a loop signal and provides an up signal when the loop signal phase lags the reference signal phase and a down signal when the loop signal phase leads the reference signal phase,

a first charge pump which provides a first current action in response to the up signal and a second current action in response to the down signal, being substantially opposed current source and current sink actions,

a second charge pump which combines a third current action with the first and second current actions to add a phase offset between the reference signal and the loop signal,

a charge accumulator which provides a frequency control signal in response to the combined first, second and third current actions of the first and second charge pumps,

an oscillator which provides an output signal at a frequency in response to the control signal and is coupled to the phase discriminator to provide the loop signal, and

an offset adjuster which varies one or more of the first, second or third current actions to vary the phase offset in accord with characteristics of the loop signal or characteristics of the output signal, or of signals associated with either signal.

6. A PLL according to claim 5 wherein the third current action is a current source or current sink action which operates substantially continuously under control of the offset adjuster.

7. A PLL according to claim 5 further including a current set which creates a common current level which determines operation of the first, second and third current actions.

8. A PLL according to claim 5 further including a controller which determines the third current action in accord with modulation of the loop signal by a frequency divider.

9. A PLL according to claim 5 further including a controller which determines the third current action to reduce noise or spurs in the output signal.

10. A phase lock loop including:

a phase discriminator which receives a reference signal and a loop signal and provides an up signal when the loop signal phase lags the reference signal phase and a down signal when the loop signal phase leads the reference signal phase,

a first charge pump which provides a first current action in response to the up signal and a second current action in response to the down signal, being substantially opposed current source and current sink actions,

a second charge pump which provides a third current action having a magnitude substantially proportional to that of the first or second current action to add a predetermined phase difference between the reference signal and the loop signal,

a charge accumulator which provides a frequency control signal in response to the combined first, second and third current actions of the first and second charge pumps, and

an oscillator which provides an output signal at a frequency in response to the control signal and is coupled to the phase discriminator to provide the loop signal.

11. A frequency synthesiser including:

a phase discriminator which receives a reference signal and a feedback signal and provides frequency adjustment signals in response to a phase difference between the reference signal and the feedback signal,

a control arrangement coupled to the discriminator which receives the frequency adjustment signals and provides an oscillator control signal,

an oscillator coupled to the control arrangement which receives the control signal and provides a synthesiser output signal at a frequency determined by the control signal, and

a frequency divider coupled between the oscillator and the discriminator which receives the synthesiser output signal and provides the feedback signal,

wherein the control arrangement is configured to produce a substantially predetermined phase difference between the feedback signal and the reference signal at the discriminator.

12. A method of linearising a phase discriminator in a frequency synthesiser including:

receiving a reference signal and a feedback signal at input to the discriminator,

generating a frequency adjustment signal in the discriminator in response to a phase difference between the reference and feedback signals,

generating an oscillator control signal in response to the phase adjustment signal,

generating a synthesiser output frequency in response to the oscillator control signal, and

coupling the synthesiser output signal to the discriminator to provide the feedback signal,

wherein the oscillator control signal is generated to produce a substantially predefined phase difference between the reference signal and the feedback signal at the input to the discriminator.

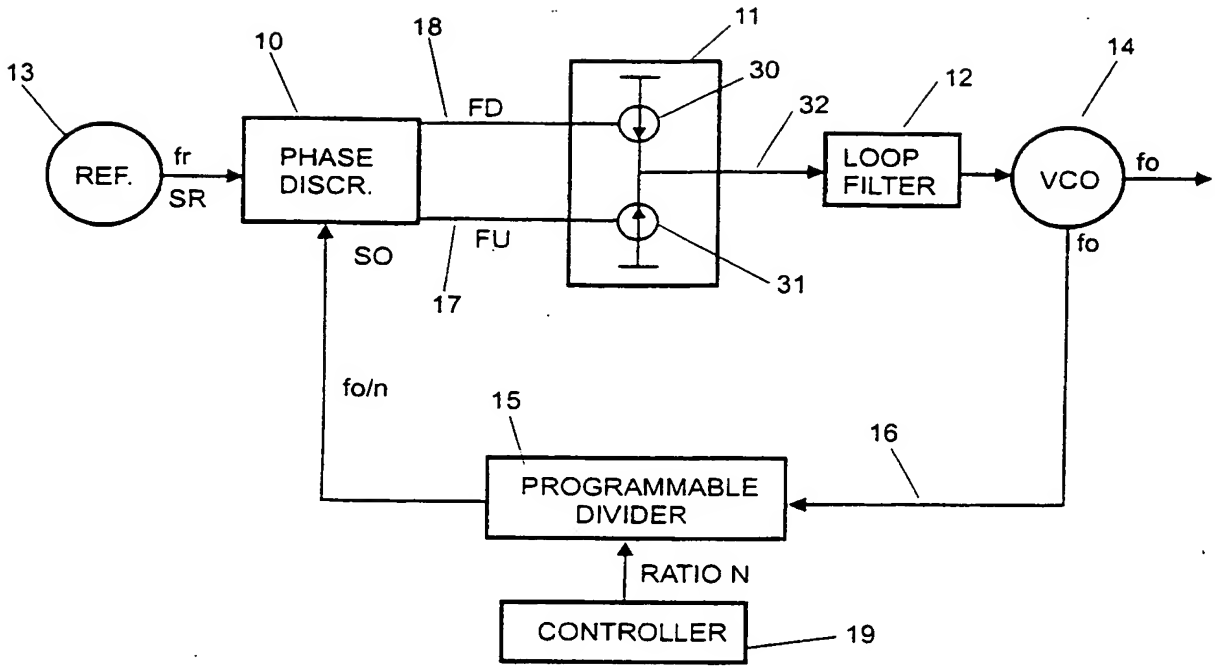

FIGURE 1

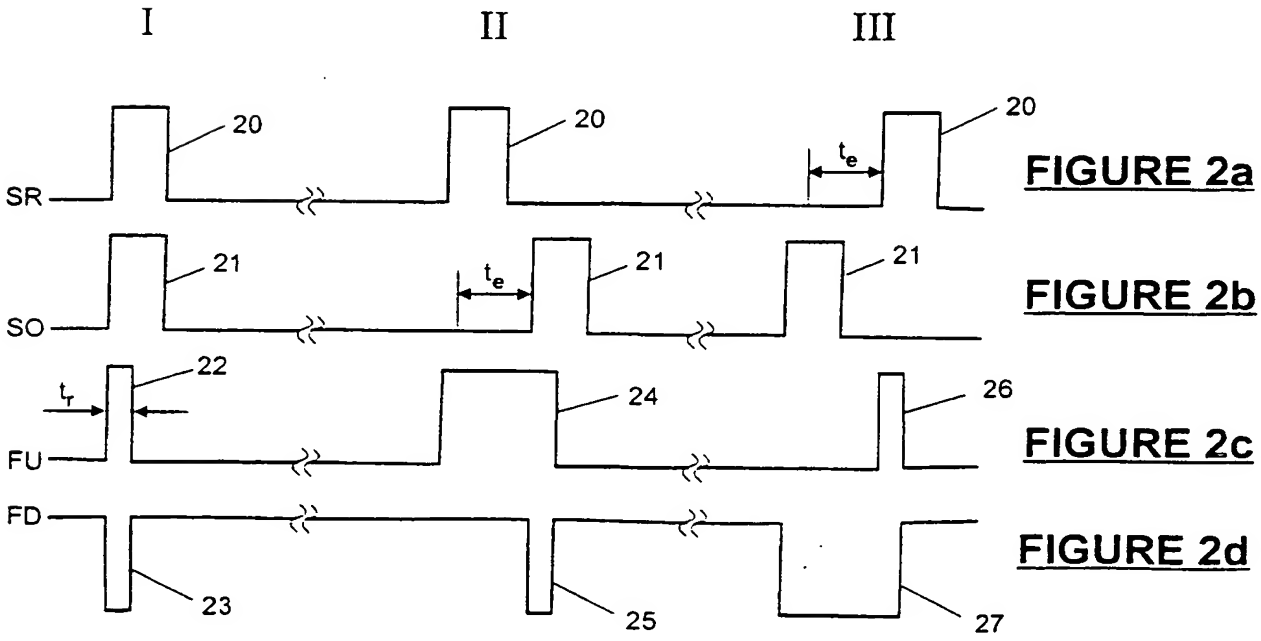

FIGURE 2a

FIGURE 2b

FIGURE 2c

FIGURE 2d

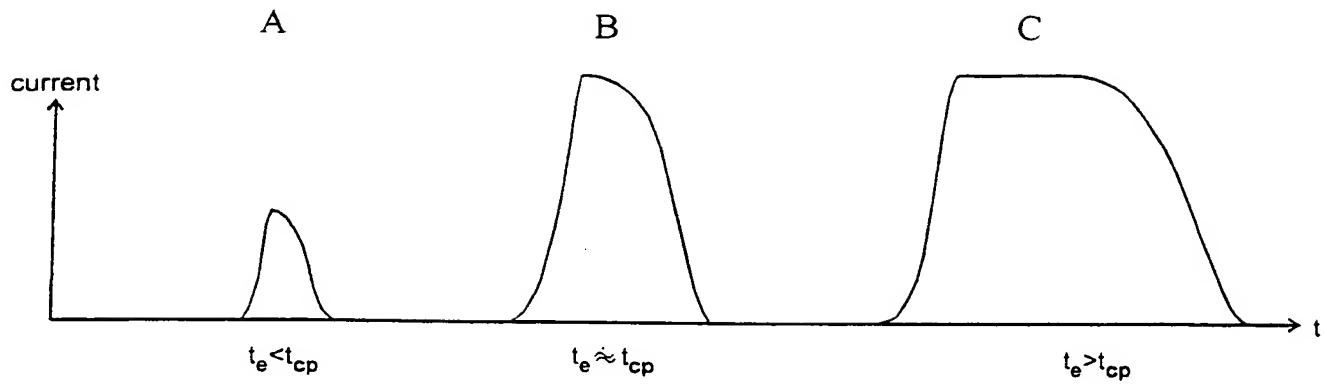

FIGURE 3

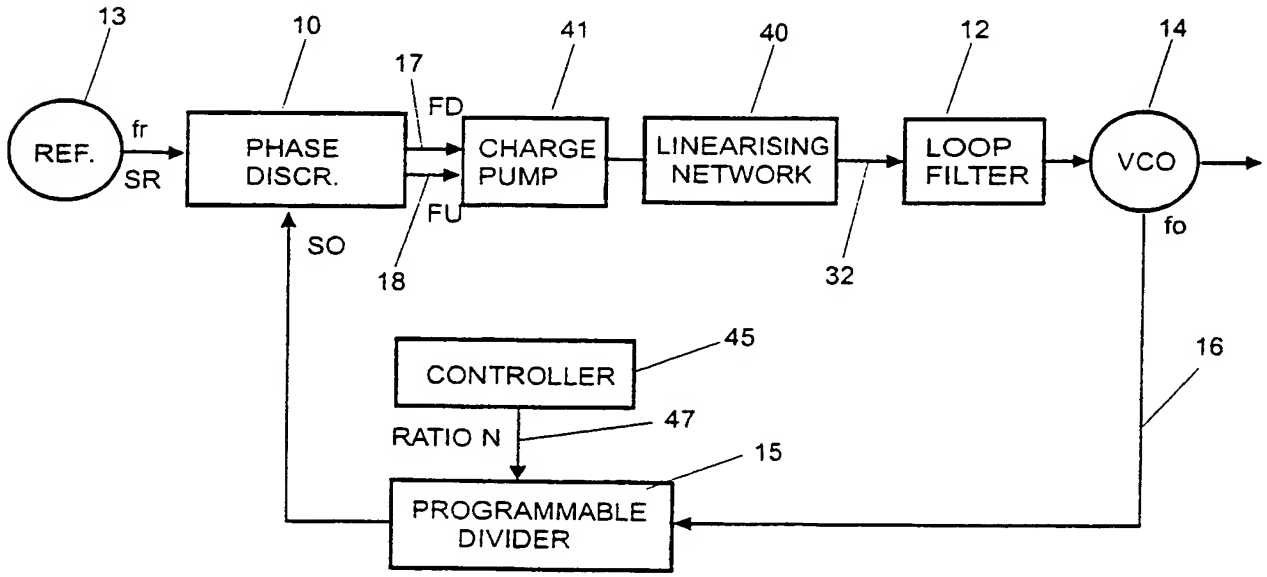

FIGURE 4a

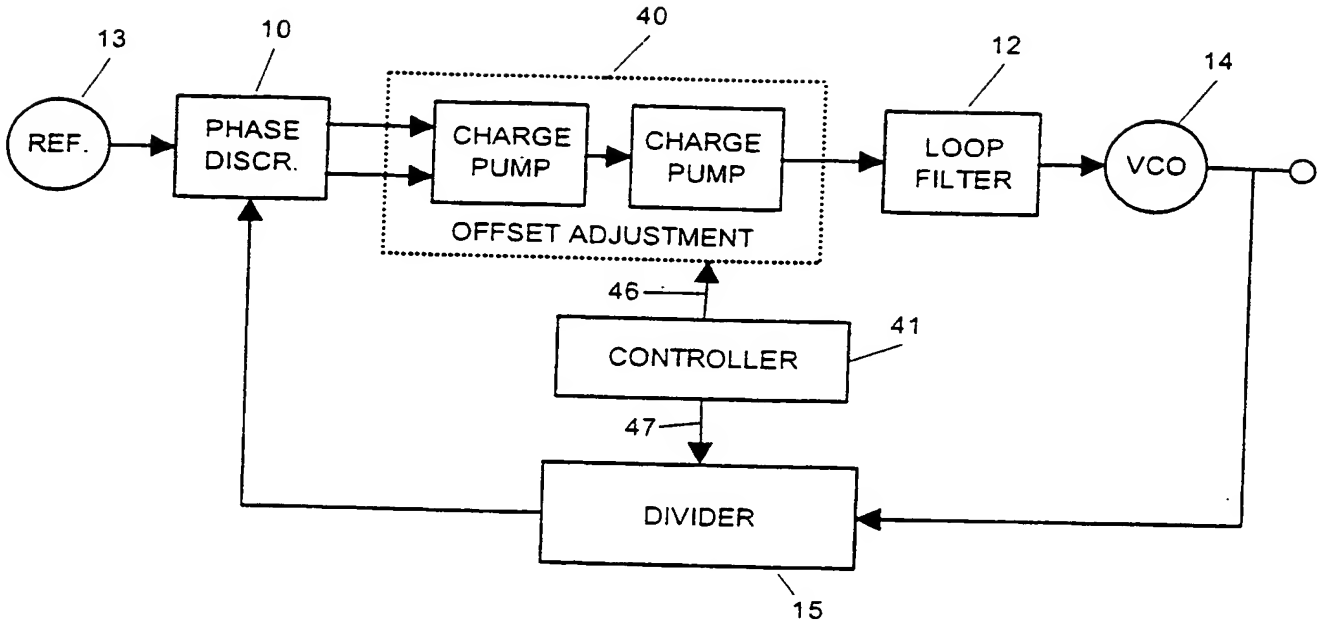

FIGURE 4b

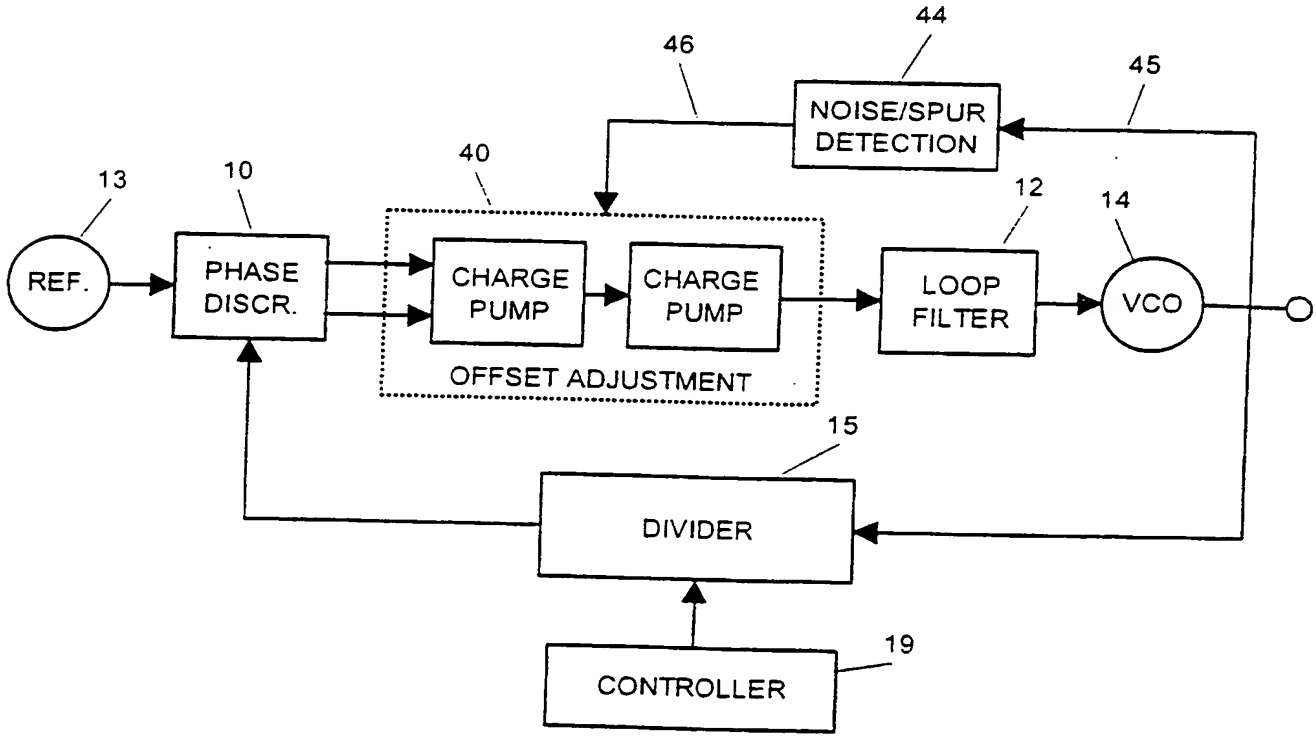

FIGURE 4c

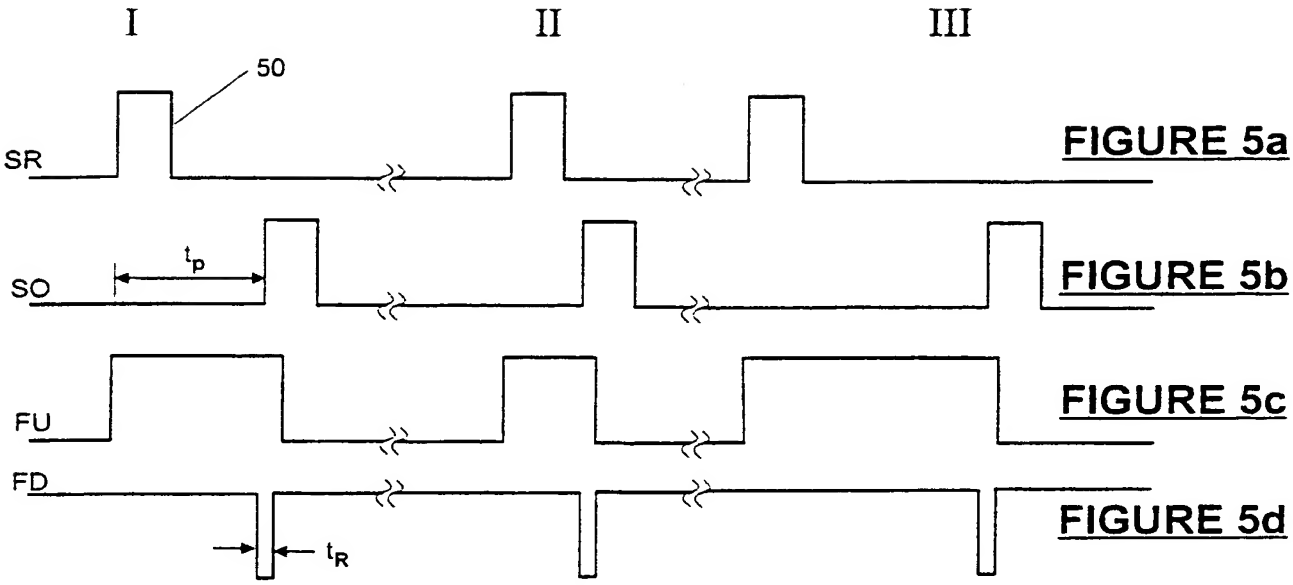

FIGURE 5a

FIGURE 5b

FIGURE 5c

FIGURE 5d

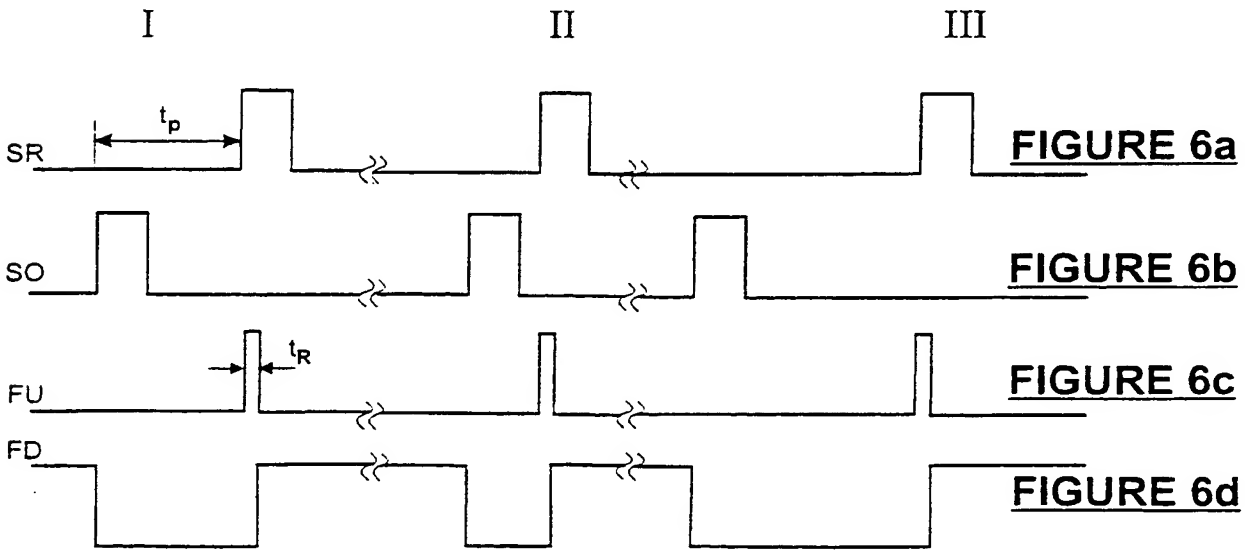

FIGURE 6a

FIGURE 6b

FIGURE 6c

FIGURE 6d

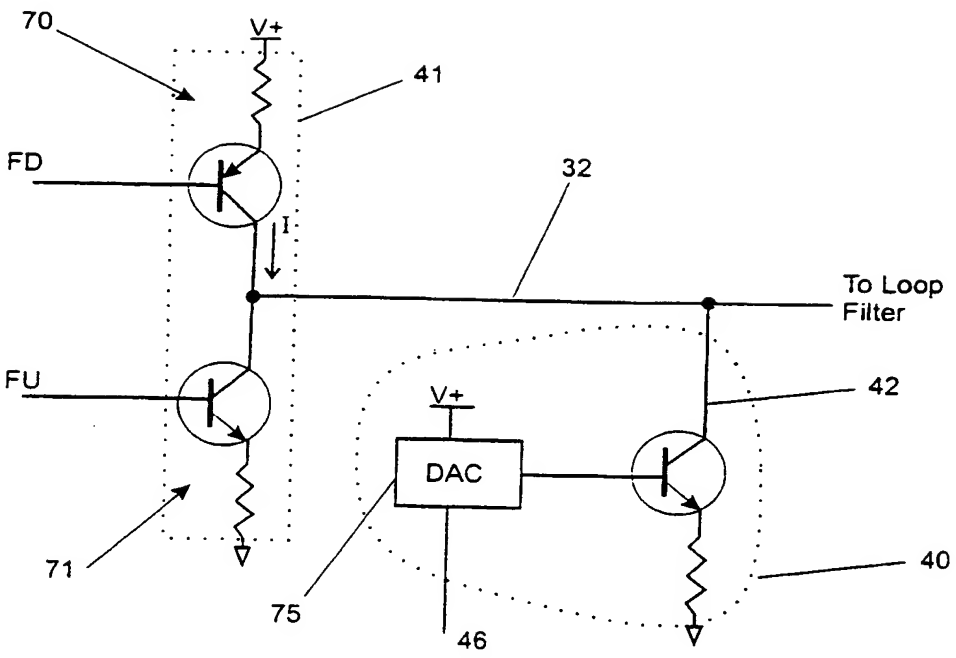

FIGURE 7

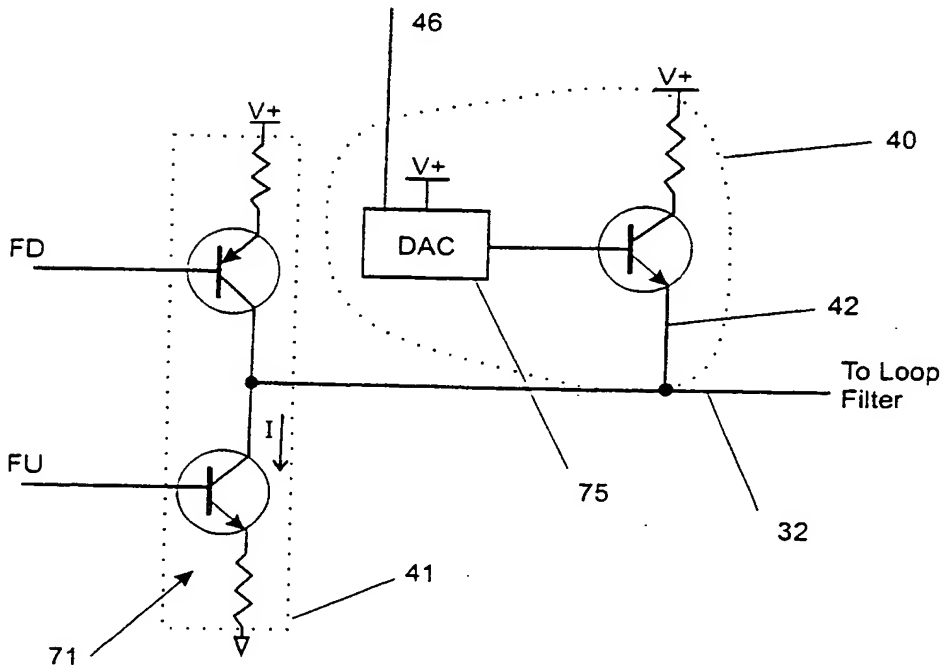

FIGURE 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NZ99/00207

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H03L 7/085, 7/089
US CL : 331/10, 17, 25

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 331/10, 11, 17, 25

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
None

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4,885,554 A (WIMMER) 05 DECEMBER 1989 (05.12.1989), column 3, line 60 to column 4, line 54, Fig. 1.	1, 4-5, 6-12
X --- Y	US 4,918,405 A (HERLEIKSON) 17 APRIL 1990 (17.04.1990), column 2, lines 38-43, column 5, line 55 to column 7, line 68, Figs. 1, 2.	1, 2, 12 ------ 3
X,P --- Y,P	US 5,940,608 A (MANNING) 17 AUGUST 1999 (17.08.1999), column 2, lines 31-34, column 3, line 5 to column 4, line 41, Fig. 3.	1, 12 ------ 3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search 29 March 2000 (29.03.2000)	Date of mailing of the international search report 17 APR 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Siegfried H. Grimm Telephone No. (703) 308-0956

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/NZ99/00207

Continuation of B. FIELDS SEARCHED Item 3: USPTO APS WEST USPT
(phase adj2 (detect$3 or discriminat$3 or compar$4)) with (((predetermined or predefined) adj2 phase difference) or phase offset) same (phase lock$3 loop or PLL or frequency synthesi?er)